# COURSE DESCRIPTION CARD - SYLLABUS

Course name
Reconfigurable and Programmable Systems [S2Teleinf2-BSiU>UR]

## Course

Field of study
Teleinformatics

Year/Semester
1/2

Area of study (specialization)
Network and service security

Profile of study
general academic

Level of study
second-cycle

Course offered in
Polish

Form of study
full-time

Requirements
compulsory

## Number of hours

Lecture
14

Laboratory classes
24

Other
14

Tutorials
0

Projects/seminars
0

## Number of credit points

3,00

## Coordinators

dr hab. inż. Olgierd Stankiewicz prof. PP
olgierd.stankiewicz@put.poznan.pl

## Lecturers

## Prerequisites

Has knowledge of programming in C/C++ / Python languages. Has knowledge of programming in HDL languages (Verilog / VHDL). Is able to obtain information from literature and databases and other sources. Knows the limitations of his/her own knowledge and skills, understands the need for further training. Able to implement team projects.

## Course objective

Learning the principles of programmable digital circuits. Combination of a processor and an FPGA (SoC - System on Chip). Learning about groups of circuits, their internal structure and functional characteristics. Learn about the stages of developing software for a SoC, designing the programmable part, configuring the processor part.

## Course-related learning outcomes

Knowledge:
K2_W07 Has basic knowledge of the development trends of SoC chips.
Knows the working principle of SoC chip, understands the principles of communication between processor and programmable parts.

K2_W10 Has an in-depth and comprehensive knowledge of the mechanisms present in the development cycle of ICT systems, in relation to both hardware and software components.
K2_W11 Is familiar with advanced methods, techniques and tools used in solving complex engineering tasks and carrying out research work in the selected area of ICT

Skills:
K2_U13 He/she is able to organise and carry out research, including experiments and computer simulations, analyse the results obtained and draw conclusions from them, and formulate and test assumptions related to complex technical issues and simple research problems.
Has sufficient knowledge to design specialized platforms implemented on SoCs.
K2_U08 Is able to separate tasks into processor and programmable parts
K2_U16 Is able to analyse the usability and implementation potential of the latest innovations (techniques and solutions) and new products in the field of ICT.
Knows how to build an application on SoC chips.

Social competences:
Is open to opportunities for continuous learning and understands the need to improve professional competence. K2_K01
Has the basic knowledge necessary to understand the non-technical conditions of engineering activities; knows the basic principles of occupational safety and health.

## Methods for verifying learning outcomes and assessment criteria

Learning outcomes presented above are verified as follows:

Lecture: written exams.
The written exam consists of 6-10 questions. A descriptive answer is expected, scored fractionally from 0 to 1 point. Passing threshold: 50% of the points.
Passing issues, on the basis of which questions are developed, will be sent to students by e-mail using the university e-mail system.
Laboratory: Laboratory project carried out individually or in small groups.

## Programme content

SoC chip design.
Overview of chip sizes from different manufacturers, basic differences between SoC chip families, more interesting chip applications.
Stages of SoC chip software preparation:
-development of the programmable part (FPGA)
-development of software for the processor part,
-prepare the operating system.
Getting acquainted with the stages of preparing a custom module in the programmable part and operating it in the processor part.

## Course topics

SoC chip design.
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-prepare the operating system.
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## Teaching methods

Lecture: multimedia presentation with examples presented on the blackboard.
Laboratories: work on computers with prepared software. Use of SoC circuits. Examples illustrated on the screen/board.

## Bibliography

Basic:
Skahill K., VHDL for Programmable Logic / Język VHDL , WNT, SBN-13: 978-0201895735, ISBN-10: 0201895730.
Giovanni De Micheli, Synthesis and Optimization of Digital Circuits / Synteza i optymalizacja układów cyfrowych , WNT, ISBN-13: 978-0070163331 ISBN-10: 0070163332.

Additional:
Łuba T., Rawski M., Tomaszewicz P., Zbierzchowski B., Synteza układów cyfrowych, Wydawnictwa Komunikacji i Łączności, Warszawa 2003.
Hajduk Z., Wprowadzenie do języka Verilog, BTC, Warszawa 2009.
Kamionka-Mikuła H., Małysiak H., Pochopień B., Synteza i analiza układów cyfrowych, WKŁ.Zbysiński P., Pasierbiński J.: Układy programowalne pierwsze kroki, Wydawnictwo BTC, Warszawa 2004,
Łuba T.. : Synteza układów logicznych. Oficyna Wyd. PW, Warszawa, 2005.

## Breakdown of average student's workload

| | Hours | ECTS |
|---|---|---|
| Total workload | 78 | 3,00 |
| Classes requiring direct contact with the teacher | 38 | 1,50 |
| Student's own work (literature studies, preparation for laboratory classes/ tutorials, preparation for tests/exam, project preparation) | 40 | 1,50 |